WHAT IS CLAIMED IS:

1. A pseudo random signal producing circuit comprising:

a first generator for generating a first pseudo random signal having a bit width a (a being an integer not smaller than 1);

a second generator for generating a second pseudo random signal having a bit width b (b being an integer not smaller than 1 and different from a);

a matrix calculator for executing a matrix calculation [operation] upon an (a, b)-type matrix with the first and the second pseudo random signals as a row and a column, respectively, to produce a calculation result signal having a bit width (a*b); and

a bit width adjusting circuit responsive to the calculation result signal having the bit width (a*b) for producing an output pseudo random signal having a bit width N (N being a divisor of (a*b)).

2. A pseudo random signal producing circuit comprising:

a first generator for generating a first pseudo random signal having a bit width a (a being an integer not smaller than 1);

a second generator for generating a second pseudo random signal having a bit width b (b being an integer not smaller than 1 and different from a);

a matrix calculator for executing a matrix calculation upon an (a, b)-type matrix with the first and the second pseudo random signals as a row and a column, respectively, to produce a calculation result signal having a bit width (a*b); and

an N-bit shift register responsive to the calculation result signal having the bit width (a*b) for producing an output pseudo random signal having a bit width N (N being a divisor of (a*b)).

3. A pseudo random signal producing circuit comprising:

a first generator for generating a first pseudo random signal having a bit width a (a being an integer not smaller than 1);

a second generator for generating a second pseudo random signal having a bit width b (b being an integer not smaller than 1 and different from a);

a matrix calculator for performing a matrix calculation upon the first and the second pseudo random signals to produce a calculation result signal having a bit width (a*b); and

a bit width adjusting circuit responsive to the calculation result signal having the bit width (a*b) for producing an output pseudo random signal having a bit width N (N being a divisor of (a*b)).

4. A pseudo random signal producing circuit comprising:

a first generator for generating a first pseudo random signal having a bit width a (a being an integer not smaller than 1);

a second generator for generating a second pseudo random signal having a bit width b (b being an integer not smaller than 1 and different from a);

a first matrix calculator for performing a matrix calculation upon an (a, b)-type matrix with the first and the second pseudo random signals as a row and a column, respectively, to produce a first calculation result signal having a bit width (a*b);

a third generator for generating a third pseudo random signal having a bit width c (c being an integer not smaller than 1 and different from a and b);

a second matrix calculator for performing a matrix calculation upon a (a*b, c)-type matrix with the first calculation result signal and the third pseudo random signal as a row and a column, respectively, to produce a second calculation result signal having a bit width (a*b*c);

and

a bit width adjusting circuit responsive to the second calculation result signal having the bit width (a*b*c) for producing an output pseudo random signal having a bit width N (N being a divisor of (a*b*c)).

5. A pseudo random signal producing circuit comprising:

a first generator for generating a first pseudo random signal having a bit width a (a being an integer not smaller than 1);

a second generator for generating a second pseudo random signal having a bit width b (b being an integer not smaller than 1 and different from a);

a first matrix calculator for performing a matrix calculation upon an (a, b)-type matrix with the first and the second pseudo random signals as a row and a column, respectively, to produce a first calculation result signal having a bit width (a*b);

a third generator for generating a third pseudo random signal having a bit width c (c being an integer not smaller than 1 and different from a and b);

a second matrix calculator for performing a matrix calculation upon a (a*b, c)-type matrix with the first calculation result signal and the third pseudo random signal as a row and a column, respectively, to produce a second calculation result signal having a bit width (a*b*c); and

an N-bit shift register responsive to the second calculation result signal having the bit width (a*b*c) for producing an output pseudo random signal having a bit width N (N being a divisor of (a*b*c)).

6. A pseudo random signal producing circuit comprising:

a first generator for generating a first pseudo random signal having a bit width a (a being an integer not smaller than 1);

a second generator for generating a second pseudo random signal having a bit width b (b being an integer not smaller than 1 and different from a);

a first matrix calculator for performing a matrix calculation upon the first and the second pseudo random signals to produce a first calculation result signal having a bit width (a*b);

a third generator for generating a third pseudo random signal having a bit width c (c being an integer not smaller than 1 and different from a and b);

a second matrix calculator (150) for performing a matrix calculation upon the first calculation result signal and the third pseudo random signal to produce a second calculation result signal having a bit width (a*b*c); and

a bit width adjusting circuit responsive to the second calculation result signal having the bit width (a*b*c) for producing an output pseudo random signal having a bit width N (N being a divisor of (a*b*c)).